

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-10 (Cancelled)

11. (Original) A semiconductor integrated circuit device which has a signal input point, a signal output point, and plural circuit blocks provided in series between the signal input point and the signal output point and in which the timings of a signal input operation from the signal input point, a signal output operation at the signal output point, and a signal transmission operation among the plural circuit blocks are respectively controlled by timing signals,

wherein, when the clock signal cycle is T_1 , the total of signal response periods of individual circuit blocks of the plural circuit blocks is T_2 , and the ratio T_2/T_1 between T_1 and T_2 is $n+\alpha$ (n is an integer and α is a positive number equal to or less than 1), a signal response period from the signal input point to the signal output point is set to $n+1$ times the clock signal cycle T_1 .

Claims 12-19 (Cancelled)

20. (Original) The semiconductor integrated circuit device according to Claim 11,

wherein said plural circuit blocks include a first circuit block and a second circuit block,

wherein said first circuit block receives a signal input in accordance with a first timing signal,

wherein said second circuit block outputs a signal output in accordance with a second timing signal,

wherein said first and second timing signals are controlled by said clock signal.

21. (Original) The semiconductor integrated circuit device according to Claim 20, further comprising:

a timing generating circuit which generates said first and second timing signals in accordance with said clock signal;

a plurality of DRAM macro cells;

a read and write buffer; and

an address decoder,

wherein said timing generating circuit includes a delay circuit which is programmable.

22. (Original) The semiconductor integrated circuit device according to Claim 21,

wherein said time difference between said first and second timing signals is other than a multiple cycle of said clock signal.

23. (Original) The semiconductor integrated circuit device according to Claim 21, further comprising:

a redundancy address setting circuit including fuses,
and

wherein said timing generating circuit includes fuses.